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(54) **Precision analog-to-digital converter with low-resolution and high-resolution conversion paths**

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Description

Background of the Invention

This invention relates generally to analog-to-digital converters, and in particular to a precision analog-to-digital converter having low-resolution and high-resolution conversion paths.

There are many conventional analog-to-digital converters that are capable of measuring analog voltages with a high degree of precision. Most of these, however, are quite sophisticated, take up a great deal of space, consume a large amount of power, and are comparatively expensive. There are some measurement situations in which it would be desirable to provide a high-resolution analog-to-digital converter using relatively simple and inexpensive parts, and capable of implementation in a small area. One such situation, for example, is measurement of low-level signals from transducers, such as pressure transducers and the like, wherein it is desired to place a high-resolution analog-to-digital converter in a small module near the transducer and remote from the measuring instrument.

US-A-4 901 078 discloses an analog-to-digital converter which is arranged first to convert an input voltage into a digital value using a high-resolution recirculating-remainder A/D converter operated as a window detector. The input scaling is adjusted on the basis of the output of the window detector. The digital conversion is then repeated. Based on the output thereof, a signal generator produces a DC voltage which differs from the scaled input voltage by about 1/100thà of the dynamic range of the window detector. This difference is amplified by a low gain difference amplifier, and the output is then delivered to the window detector to produce a further digital value, which is combined with the value used to generate the DC voltage in order to obtain a representation of the input voltage.

Summary of the Invention

Aspects of the present invention are set out in the accompanying claims.

In one embodiment, a comparatively low-resolution (e.g., 4 bits or 8 bits) analog-to-digital converter (ADC) first converts an input signal to digital form to provide a first measurement. A first converted voltage for a 4-bit ADC is within 6.25% of the actual value of the input signal; for an 8-bit ADC, the converted voltage is within 0.4% of the actual value of the input signal. This value is utilized to establish the output DC voltage of a programmable precision DC voltage source, which DC voltage is applied to one input of a high-gain operational amplifier operated as a null detector, while the input signal is applied to the other input thereof. The sensitivity of the null detector is such that its output will be locked to one of its dynamic operating range limits, or saturated, if the voltage difference at its two inputs exceeds a predetermined voltage. In a preferred embodiment, a microprocessor stores the first-converted value, and then, using an 8-bit ADC, controls the duty cycle of a square-wave voltage signal that is applied to a low-pass filter to produce a pulse-width modulated direct-current (DC) voltage. That is, the precision DC voltage source produces a pulse-width-modulated DC voltage for application to one input of the high-gain operational amplifier. The gain of the operational amplifier is 500 so that the sensitivity is 20 millivolts for a 10-volt output swing (+5 V to -5 V).

Initially, the null detector is saturated, and its output voltage is clamped to a positive or negative supply voltage rail. The duty cycle of the switching signals is altered by the microprocessor to change the pulse-width modulated DC voltage until it is sufficiently close to the input signal to bring the null detector out of saturation and bring its output voltage within the dynamic operating range of the operational amplifier.

A binary search technique may be employed to adjust the duty cycle to locate a pulse-width modulated voltage which will either cause the null detector to come out of saturation or will be sufficiently close that a slight alteration in the duty cycle may be made to cause the null detector to come out of saturation. Alternatively, the first-converted value can be utilized to program a programmable counter to establish an initial duty cycle that can subsequently be varied one bit at a time until a pulse-width modulated voltage that causes the null detector to come out of saturation is reached. The first-converted value may be used to predict what the pulse-width modulated DC voltage should be so that the time taken to get the high-resolution measurement is slightly longer than the settling time of the pulse-width modulation circuit. Thus, the null detector comes out of saturation almost as soon as a pulse-width modulated DC voltage is developed, or after a few duty cycle adjustments, and output voltage thereof then may be converted to digital form to provide a second measurement, again using a low-resolution analog-to-digital converter. The output voltage of the null detector for the second measurement is between 0% and 0.4% of the input signal value when measured with an eight-bit analog-to-digital converter, as it was for the first measurement, and when added to the first-converted value (or a modified first-converted value used to establish the final duty cycle), yields a final value measured with an effective resolution of 18 to 22 bits of accuracy.

A preferred embodiment of the present invention is implemented in a measurement instrument for monitoring the analog voltage obtained from a commercially available pressure transducer. Signal conditioning is achieved using a precision instrumentation amplifier to match the output voltage range of the transducer with the measurement circuitry. A microprocessor including a simple 8-bit ADC is multiplexed between a low resolution (but high speed) reading and a fully settled reading of the null detector, which is rather slow, but produces 18 to 22 bits of accuracy. The low-resolution reading is displayed to a user via a display device to give an indication of the measured input signal if the input signal is too noisy for the slower conversion to converge. A complete converged measurement process takes about a half a second to yield a high-resolution output, and can automatically sample and update the readings on a periodic basis.

The present invention can provide a simple, compact, low-cost, high-performance sampling analog-to-digital converter having a high-speed, low resolution conversion path, and a low-speed, high resolution conversion path.

Brief Description of the Drawings

Fig. 1 is a generalized block diagram of an analog-to-digital converter in accordance with the present invention;

Fig. 2 is a block diagram of a preferred embodiment of the present invention;

Figs. 3A - 3C are waveforms to explain the operation of the pulse-width modulation technique employed by the preferred embodiment of the present invention; and

Fig. 4 is a schematic diagram of a preferred embodiment of the present invention.

Detailed Description of the Invention

Referring to Fig. 1 of the drawings, a generalized block diagram of an analog-to-digital converter (ADC) in accordance with the present invention is shown in which an input analog voltage to be measured is applied via an input terminal 10 to a signal conditioning circuit 12. Signal conditioning circuit 12 may be any conventional amplifier or attenuator, or a combination thereof, to condition and scale the input signal voltage to a suitable level for measurement within the conversion window or input range of the ADC.

The conditioned input voltage is applied to a comparatively low-resolution ADC 14, where it is converted to a digital representation. ADC 14 may be a simple 4-bit or 8-bit converter for first converting the input voltage to digital form to provide a first-converted voltage measurement. The first converted voltage for a 4-bit ADC is within 6.25% of the actual value of the input voltage; for an 8-bit ADC, the converted voltage is within 0.4% of the actual value of the input voltage.

A microprocessor 16 reads the output of ADC 14 and transports the digital representation of the amplitude, plus polarity sign, over a conventional microprocessor bus structure 18 to a memory device 20, which may suitably include a random-access memory (RAM) as well as a read-only memory (ROM) for storing programmed instructions, and to a display device 22, where it is immediately available to a user. Display device 22 may be any of a number of conventional display devices, such as a flat panel liquid crystal display (LCD) or the like.

Microprocessor 16 also initiates a programmable precision DC voltage generator 24, which may suitably be any of a number of well known programmable voltage sources, such as a digital-to-analog converter. The digital representation of the input voltage may be used by microprocessor 16 to initiate the voltage generator 24 to immediately produce a DC voltage near the input voltage being measured. The DC voltage is applied to one input of a null detector 30, which may be a high-gain operational amplifier, while the input signal is applied to the other input thereof. The output of null detector 30 is applied to a second ADC 32, which may be identical to ADC 14.

Initially, the null detector 30 is saturated, and its output voltage is clamped to a positive or negative supply voltage rail, such as +5 volts and -5 volts, which are the limits of its dynamic operating range. Microprocessor 16 reads the output of ADC 32, which indicates the saturated state of null detector 30, and alters the programming data applied over bus 18 to the precision DC voltage generator to change the DC voltage applied to null detector 30 until it is sufficiently close to the input voltage to bring null detector 30 out of saturation and bring its output voltage within the dynamic operating range of the operational amplifier.

Microprocessor 16 detects the unsaturated state of null detector 30 via ADC 32 and reads the second converted digital representation. The gain of the operational amplifier in null detector 30 may be such that the output voltage window provided by null detector 30 can interpolate

between discrete conversion levels of ADC 14. This situation permits simply adding the second reading provided by ADC 32 to the first reading provided by ADC 14 to produce a final value. In any case, the programmed DC voltage, known to microprocessor 16 which caused such voltage to be generated, is added to the value measured by ADC 32 to provide a very precise representation of the unknown input voltage, with an effective resolution of 18 to 22 bits of accuracy. The final value then may be displayed to the user by display device 22. The final reading may take about a half a second to obtain, and can be updated on a periodic basis, for example, every second.

The first-converted value may be used to predict what the programmable DC voltage should be, and accordingly utilized to initialize the programmable precision DC voltage generator 24. Thereafter, a binary search technique may be employed to adjust the program data applied to voltage generator 24 to locate a DC voltage which will cause null detector 30 to come out of saturation. Alternatively, the program data can be varied one bit at a time until a DC voltage that causes null detector 30 to come out of saturation is reached. Thus, null detector 30 comes out of saturation almost as soon as a DC voltage is developed, or after a few adjustments, and the output voltage thereof then may be converted to digital form to provide a second conversion measurement, again using a low-resolution analog-to-digital converter. The output voltage of the null detector for the fine measurement is between 0% and 0.4% of the input signal value when measured with an eight-bit analog-to-digital converter, and when added to the first-converted value (or a modified first-converted value used to establish the final duty cycle), yields a final value measured with an effective resolution of 18 to 22 bits of accuracy.

A preferred embodiment of the present invention is shown in block diagram form in Fig. 2, wherein like reference numerals are used for like elements. Here, the precision DC voltage source 24 is replaced by a duty-cycle control circuit 26 which controls the duty cycle of a square-wave voltage signal that is applied to a low-pass filter in a pulse-width modulation circuit 28 to produce a pulse-width modulated direct-current (DC) voltage. The rest of the circuit elements operate substantially as described in connection with Fig. 1. Again, as discussed above in connection with Fig. 1, the digital representation of the input voltage may be used by microprocessor 16 to initiate the duty-cycle control circuit 24 to immediately approximate a pulse-width modulated DC voltage near the input voltage being measured. The pulse-width-modulated DC voltage is applied to one input of a high-gain operational amplifier of null detector 30, while the input signal is applied to the other input thereof. The null detector 30 operates as described above. The duty cycle of the switching signals is altered by the microprocessor 16 to change the pulse-width modulated DC voltage applied to null detector 30 until it is sufficiently close to the input voltage to bring null detector 30 out of saturation and bring its output voltage within the dynamic operating range of the operational amplifier.

The first-converted value may be used to predict what the pulse-width modulated DC voltage should be, and accordingly utilized to initialize the duty cycle. Thereafter, a binary search technique may be employed to adjust the duty cycle to locate a pulse-width modulated voltage which will cause null detector 30 to come out of saturation. Alternatively, the first-converted value can be utilized to program a programmable counter to establish an initial duty cycle that can subsequently be varied one bit at a time until a pulse-width modulated voltage that causes null detector 30 to come out of saturation is reached. In any case, the pulse-width modulated DC voltage can be adjusted very precisely and quickly by varying the duty cycle of the control signal. Thus, null detector 30 comes out of saturation almost as soon as a pulse-width

modulated DC voltage is developed, or after a few duty cycle adjustments, and the output voltage thereof then may be converted to digital form to provide a second conversion measurement, again using a low-resolution analog-to-digital converter. The output voltage of the null detector for the fine measurement is between 0% and 0.4% of the input signal value when measured with an eight-bit analog-to-digital converter, and when added to the first-converted value (or a modified first-converted value used to establish the final duty cycle), yields a final value measured with an effective resolution of 18 to 22 bits of accuracy.

To gain an appreciation of how the pulse-width modulated DC voltage is developed by adjusting the duty cycle of a square-wave signal, refer to the waveform diagrams shown in Figs. 3A through 3C. In Fig. 3A, a square-wave signal 40 is shown having an amplitude that varies from zero volts (0 V) to an exemplary reference voltage of five volts (+5 V), and has a duty cycle of 50%. That is, over one cycle indicated by time T, the square-wave voltage is at +5 V one-half of the time, or ½T, and at 0 V one-half of the time, or ½T. When filtered, a pulse-width modulated DC voltage level 42 is produced which is equal to one-half of the amplitude of the square-wave voltage, or +2.5 volts. In Fig. 3B, the duty cycle is adjusted to 25%, so that the square-wave signal voltage is at +5 V one-fourth of the time (¼T) and at 0 V three-fourths of the time ('T), resulting in a pulse-width modulated DC voltage of +1.25 V. Similarly, in Fig. 3C, the duty cycle is adjusted to 75%, so that the square-wave signal voltage is at +5 V three-fourths of the time ('T) and at 0 V one-fourth of the time (¼T), resulting in a pulse-width modulated DC voltage of +3.75 V. Thus, it can be discerned that the pulse-width modulated DC voltage 42 is proportional to the duty cycle of the control signal 40. For example, if a binary search sequence is used to adjust the pulse-width modulated DC voltage 42, the duty cycle may be first set to 50%, or to a percentage proportional to the value of the first reading by ADC 14, then the output of null detector 30 read to determine its state. Thereafter, the duty cycle can be adjusted to develop a pulse-width modulated DC voltage that converges toward the voltage of the input voltage in a well-known binary sequence V±½V±¼V±1/8V,etc., until the output of the null detector 30 comes out of saturation. It should be pointed out that while a positive polarity is used in this example, the principles described herein are identical for negative-polarity voltages.

Fig. 4 shows a preferred embodiment of the present invention as implemented to monitor the analog voltage from a commercially available pressure transducer 50 connected between a reference voltage of +5 V and ground. Pressure transducer 50 may be monitoring air pressure in an air line, for example. As pressure varies, a differential voltage is developed across internal resistances and applied to a signal conditioning stage comprising a precision instrumentation amplifier 52. Instrumentation amplifier 52 is configured as an operational amplifier to match the output range of the transducer with the measurement circuitry to condition the input signal, and in this embodiment has an output dynamic range of +5 volts to -5 volts. Resistors 54-57 associated with instrumentation amplifier 52 in this embodiment were selected to provide a gain of 40 for the signal conditioning stage.

The output of instrumentation amplifier 52, which is a replication of the input voltage, is applied directly to a microprocessor 60, which couples the replicated input voltage to an internal 8-bit ADC 62 via a multiplexer 64. One microprocessor capable of performing the functions described herein is a Hitachi H8-327 microprocessor. A duty-cycle control circuit 66, which may suitably be a variable duty cycle flip flop, provides complementary control signals at a one-kilohertz rate to operate a pair of switches 70 and 72, which alternately connect one end

of a resistor 74 to a precise +5 V or -5 V reference, depending on the polarity of the input voltage, and ground in order to generate a square wave voltage similar to that shown in Figs. 3A-3C. Resistor 74 and capacitor 76 form a low-pass filter which effectively integrates the square-wave voltage to produce a pulse-width modulated DC voltage as described hereinabove.

The pulse-width modulated DO voltage generated by resistor 74 and capacitor 76 is applied to one input of an operational amplifier 80 that is operated as a null detector. The output of instrumentation amplifier 52 is coupled to a second input of operational amplifier 80 via an input resistor 82. A gain-setting feedback resistor 84 coupled from the output of operational amplifier 80 to its second input completes the null detector, and resistors 82 and 84 are selected to provide a gain of 500. Thus the sensitivity of the null detector is very high, and a 20 millivolt difference between the two inputs thereof will result in 10-volt change in the output. Since the output limits of the null detector are +5 volts and -5 volts, an input difference of greater than 20 millivolts will saturate the null detector and hold the output at one of the two extremes. The output of the null detector or operational amplifier 80 is coupled via mulitiplexer 64 to ADC 62. Thus, a single ADC 62 may be used for both the low-resolution, or first reading and the high-resolution, or second reading. Otherwise, the overall circuit functions as described hereinabove, and microprocessor 60 including a simple 8-bit ADC 62 is multiplexed between a low resolution (but high speed) reading and a fully settled reading of the null detector, which is rather slow, but produces 18 to 22 bits of accuracy. The low-resolution reading is available immediately to a user via a display device to give an indication of the measured input signal while the slower conversion is taking place. The entire process takes about a half a second to yield a high-resolution output, and the system can automatically sample and update the readings on a periodic basis.

Claims

1. A voltage measurement circuit comprising:

an input path for receiving an input voltage to be measured;

analog-to-digital conversion means (14,32; 62) arranged for converting the input voltage to a first converted voltage;

a processor circuit (16; 60) arranged for receiving said first converted voltage;

a programmable DC voltage generator (24; 26,28; 66,70,72,74,76) arranged to provide a DC reference voltage having a level determined by the processor circuit (16; 60) the processor circuit (16; 60) determining a starting level from said first converted voltage;

difference means (30; 80,82,84) having a first input coupled to said input path, a second input coupled to an output of said programmable DC voltage generator (24; 26,28; 66,70, 72,74,76) and an output coupled to said analog-to-digital conversion means (14,32; 62), the difference means (30; 80,82,84) being operable to provide at its output a difference signal representing the difference between the levels at its inputs, and the analog-to-digital conversion means (14,32; 62) being operable to convert the difference signal to a second converted voltage;

said processor circuit (16; 60) being operable to combine the second converted voltage with the first converted voltage used to provide the DC reference voltage to provide a final converted voltage representative of said input voltage;

characterised in that:

said difference means comprises a null detector (30; 80,82,84) which provides said difference signal only when the voltages at its first and second inputs are substantially equal; and

said processor circuit (16; 60) is arranged to monitor an output of the analog-to-digital converter means (14,32; 62) while altering the first converted voltage to command the programmable DC voltage generator (24; 26,28; 66,70,72,74,76) to adjust said DC reference voltage until the output of said null detector (30; 80,82,84) indicates that the voltages at its first and second inputs are substantially equal.

2. A voltage measurement circuit in accordance with claim 1 wherein said processor circuit is operable to perform a binary search to establish a value for said DC reference voltage.

3. A voltage measurement circuit in accordance with claim 1 or 2 wherein said analog-to-digital conversion means is a single analog-to-digital converter (62) selectively coupled to said input path and said output of said null detector (80,82,84).

4. A voltage measurement circuit in accordance with claim 1 or 2 wherein said analog-to-digital conversion means comprises a first analog-to-digital converter (14) coupled to said input path and a second analog-to-digital converter (32) coupled to the output of said null detector.

5. A voltage measurement circuit in accordance with any preceding claim wherein said first converted voltage and said final converted voltage are provided to a display device (22).

6. A voltage measurement circuit in accordance with any preceding claim wherein said programmable DC voltage generator comprises a pulse width modulation circuit (28; 70,72, 74,76) which produces said DC reference voltage in response to a square-wave voltage signal, and further wherein said processor (16; 60) varies the duty cycle of said square-wave voltage signal.

7. A voltage measurement circuit in accordance with any preceding claim wherein said null detector is an operational amplifier (80) having a predetermined gain.

8. A method of converting an input voltage to a digital signal, the method comprising performing an initial conversion of said input voltage to obtain a first, relatively low-resolution digital value, using said first digital value to generate a corresponding analog voltage, comparing the input voltage with said analog voltage and converting the difference therebetween to a second digital value, and providing a third, relatively high-resolution

digital value as a representation of the input voltage;

characterised by the step of adjusting the first digital value until the comparison of the input voltage with the analog voltage indicates that they are substantially equal, the third digital value being based on the combination of the adjusted first digital value and the second digital value.

Patentansprüche

1. Spannungsmeßschaltung mit

einem Eingangsweg zum Empfang einer zu messenden Eingangsspannung,

einer Analog-Digital-Umwandlungseinrichtung (14, 32; 62) zur Umwandlung der Eingangsspannung in eine erste umgewandelte Spannung,

einer Verarbeitungseinheit (16; 60) zum Empfang der ersten umgewandelten Spannung,

einer programmierbaren Gleichspannungserzeugungseinrichtung (24; 26, 28; 66, 70, 72, 74, 76) zur Bereitstellung einer Gleichspannung-Referenzspannung mit einem durch die Verarbeitungsschaltung (16; 60) bestimmten Pegel, wobei die Verarbeitungsschaltung (16; 60) einen Startpegel von der ersten umgewandelten Spannung bestimmt,

einer Differenzeinrichtung (30; 80, 82, 84) mit einem ersten Eingangsanschluß, der an den Eingangsweg angeschlossen ist, einem zweiten Eingangsanschluß, der an einen Ausgangsanschluß der programmierbaren Gleichspannungserzeugungseinrichtung (24; 26, 28; 66, 70, 72, 74, 76) angeschlossen ist, und einem Ausgangsanschluß, der an die Analog-Digital-Umwandlungseinrichtung (14, 32; 62) angeschlossen ist, wobei die Differenzeinrichtung (30; 80, 82, 84) zur Bereitstellung eines Differenzsignals an ihrem Ausgangsanschluß betreibbar ist, das die Differenz zwischen den Pegeln an ihren Eingangsanschlüssen darstellt, und die Analog-Digital-Umwandlungseinrichtung (14, 32; 62) zur Umwandlung des Differenzsignals in eine zweite umgewandelte Spannung betreibbar ist,

wobei die Verarbeitungsschaltung (16; 60) zur Kombinierung der zweiten umgewandelten Spannung mit der ersten umgewandelten Spannung, die zur Bereitstellung der Gleichspannung-Referenzspannung verwendet wird, betreibbar ist, damit eine umgewandelte Endspannung bereitgestellt wird, die die Eingangsspannung darstellt,

dadurch gekennzeichnet, daß

die Differenzeinrichtung eine Null-Erfassungseinheit (30; 80, 82, 84) aufweist, die das Differenzsignal lediglich dann bereitstellt, wenn die Spannungen an ihren ersten und zweiten Eingangsanschlüssen im wesentlichen gleich sind, und

die Verarbeitungsschaltung (16, 60) eingerichtet ist, ein Ausgangssignal der Analog-

Digital-Umwandlungseinrichtung (14, 32; 62) zu überwachen, während die erste umgewandelte Spannung verändert wird, damit die programmierbare Gleichspannungserzeugungseinrichtung (24; 26, 28; 66, 70, 72, 74, 76) angewiesen wird, die Gleichspannung-Referenzspannung anzupassen, bis das Ausgangssignal der Null-Erfassungseinheit (30; 80, 82, 84) anzeigt, daß die Spannungen an ihren ersten und zweiten Eingangsanschlüssen im wesentlichen gleich sind.

2. Spannungsmeßschaltung nach Anspruch 1, wobei die Verarbeitungsschaltung zur Ausführung einer binären Suche zur Bildung eines Werts für die Gleichspannung-Referenzspannung betreibbar ist.

3. Spannungsmeßschaltung nach Anspruch 1 oder 2, wobei die Analog-Digital-Umwandlungseinrichtung eine einzelne Analog-Digital-Umwandlungseinheit (62) ist, die selektiv an den Eingangsweg und den Ausgangsanschluß der Null-Erfassungseinheit (80, 82, 84) angeschlossen wird.

4. Spannungsmeßschaltung nach Anspruch 1 oder 2, wobei die Analog-Digital-Umwandlungseinrichtung eine erste Analog-Digital-Umwandlungseinheit (14), die an den Eingangsweg angeschlossen ist, und eine zweite Analog-Digital-Umwandlungseinheit (32) umfaßt, die an den Ausgangsanschluß der Null-Erfassungseinheit angeschlossen ist.

5. Spannungsmeßschaltung nach zumindest einem der vorhergehenden Ansprüche, wobei die erste umgewandelte Spannung und die umgewandelte Endspannung bei einer Anzeigevorrichtung (22) bereitgestellt werden.

6. Spannungsmeßschaltung nach zumindest einem der vorhergehenden Ansprüche, wobei die programmierbare Gleichspannungserzeugungseinrichtung eine Impulsbreitenmodulationsschaltung (28; 70, 72, 74, 76) aufweist, die die Gleichspannung-Referenzspannung in Reaktion auf ein Rechteckspannungssignal erzeugt, und ferner die Verarbeitungsschaltung (16; 60) das Tastverhältnis des Rechteckspannungssignals variiert.

7. Spannungsmeßschaltung nach zumindest einem der vorhergehenden Ansprüche, wobei die Null-Erfassungseinheit ein Operationsverstärker (80) mit einer vorbestimmten Verstärkung ist.

8. Verfahren zum Umwandeln einer Eingangsspannung in ein digitales Signal, mit den Schritten Ausführen einer Anfangsumwandlung der Eingangsspannung, damit ein erster digitaler Wert mit relativ niedriger Auflösung erhalten wird, Verwenden des ersten digitalen Werts zur Erzeugung einer entsprechenden analogen Spannung, Vergleichen der Eingangsspannung mit der analogen Spannung sowie Umwandeln der Differenz zwischen den Spannungen in einen zweiten digitalen Wert und Bereitstellen eines dritten digitalen Werts mit relativ hoher Auflösung als Darstellung der Eingangsspannung, gekennzeichnet durch einen Schritt zum Anpassen des ersten digitalen Werts, bis der Vergleich der Eingangsspannung mit der analogen Spannung anzeigt, daß sie im wesentlichen gleich sind, wobei der dritte digitale Wert auf der

Kombination des angepaßten ersten digitalen Werts und des zweiten digitalen Werts beruht.

Revendications

1. Circuit de mesure de tension comprenant :

un trajet d'entrée destiné à la réception d'une tension d'entrée à mesurer ;

un moyen de conversion analogique-numérique (14, 32 ; 62) disposé de manière à convertir la tension d'entrée en une première tension convertie ;

un circuit processeur (16 ; 60) disposé de manière à recevoir ladite première tension convertie ;

un générateur de tension continue programmable (24 ; 26, 28 ; 66, 70, 72, 74, 76), disposé de manière à produire une tension de référence continue ayant un niveau déterminé par le circuit processeur (16 ; 60), le circuit processeur (16 ; 60) déterminant un niveau de départ de ladite première tension convertie ;

un moyen de différence (30 ; 80, 82, 84) ayant une première entrée couplée audit trajet d'entrée, une seconde entrée couplée à une sortie dudit générateur de tension continue programmable (24 ; 26, 28 ; 66, 70, 72, 74, 76) et une sortie couplée audit moyen de conversion analogique-numérique (14, 32 ; 62), le moyen de différence (30 ; 80, 82, 84) étant activable afin de produire sur sa sortie un signal différentiel représentant la différence entre les niveaux de ses sorties et le moyen de conversion analogique-numérique (14, 32 ; 62) étant activable afin de convertir le signal de différence en une seconde tension convertie ;

ledit circuit processeur (16 ; 60) étant activable afin de combiner la seconde tension convertie avec la première tension convertie servant à produire la tension de référence continue afin de produire une tension finale convertie représentative de ladite tension d'entrée ;

caractérisé en ce que :

ledit moyen de différence comprend un détecteur de zéro (30 ; 80, 82, 84) ne produisant ledit signal de différence que lorsque les tensions de ses première et seconde entrées sont pratiquement égales ; et

ledit circuit processeur (16 ; 60) est disposé afin de surveiller une sortie du moyen de conversion analogique-numérique (14, 32 ; 62) tout en modifiant la première tension convertie pour commander le générateur de tension continue programmable (24 ; 26, 28 ; 66, 70, 72, 74, 76) afin d'ajuster ladite tension de référence continue jusqu'à ce que la sortie dudit détecteur de zéro (30 ; 80, 82, 84) indique que les tensions de ses première et seconde entrées sont pratiquement égales.

2. Circuit de mesure de tension selon la revendication 1 dans lequel ledit circuit processeur est activable pour procéder à une recherche binaire afin d'établir une valeur pour ladite tension de référence continue.

3. Circuit de mesure de tension selon la revendication 1 ou 2, dans lequel ledit moyen de conversion analogique-numérique est un convertisseur analogique-numérique unique (62) couplé de manière sélective audit trajet d'entrée et à ladite sortie dudit détecteur de zéro (80, 82, 84).

4. Circuit de mesure de tension selon la revendication 1 ou la revendication 2 dans lequel ledit moyen de conversion analogique-numérique comprend un premier convertisseur analogique-numérique (14) couplé audit trajet d'entrée et un second convertisseur analogique-numérique (32) couplé à la sortie dudit détecteur de zéro.

5. Circuit de mesure de tension selon l'une quelconque des revendications précédentes dans lequel ladite première tension convertie et ladite tension finale convertie sont appliquées à un dispositif d'affichage (22).

6. Circuit de mesure de tension selon l'une quelconque des revendications précédentes, dans lequel ledit générateur de tension continue programmable comprend un circuit de modulation de largeur d'impulsion (28 ; 70, 72, 74, 76) produisant ladite tension de référence continue en réponse à un signal de tension de forme carrée, et dans lequel, en outre, ledit processeur (16 ; 60) fait varier le cycle du rapport cyclique dudit signal de tension de forme carrée.

7. Circuit de mesure de tension selon l'une quelconque des revendications précédentes dans lequel ledit détecteur de zéro est un amplificateur opérationnel (80) de gain prédéterminé.

8. Procédé de conversion d'une tension d'entrée en un signal numérique, le procédé comprenant la mise en oeuvre d'une conversion initiale de ladite tension d'entrée afin d'obtenir une première valeur numérique de résolution relativement faible, l'utilisation de la dite première valeur numérique pour générer une tension analogique correspondante, la comparaison de la tension d'entrée à ladite tension analogique et la conversion de leur différence en une seconde valeur numérique et la production d'une troisième valeur de résolution relativement élevée comme représentation de la tension d'entrée ;

caractérisé par l'étape d'ajustement de la première valeur numérique jusqu'à ce que la comparaison de la tension d'entrée avec la tension analogique indique qu'elles sont pratiquement égales, la troisième valeur numérique étant basée sur la combinaison de la première valeur numérique ajustée et de la seconde valeur numérique.

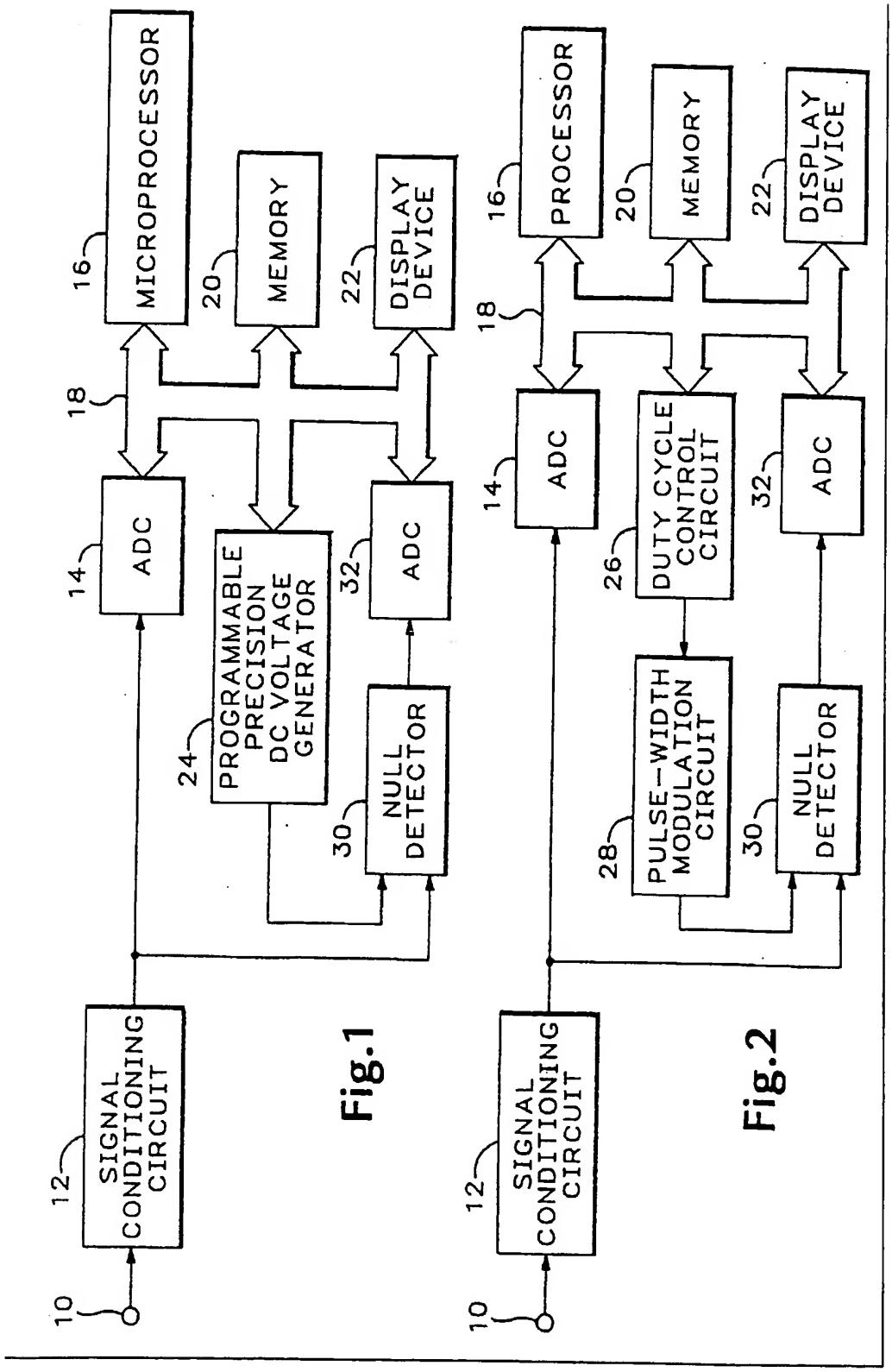
10
12
SIGNAL CONDITIONING CIRCUIT
14
ADC
16
MICROPROCESSOR
18
20
MEMORY
22
DISPLAY DEVICE
24
PROGRAMMABLE PRECISION DC VOLTAGE GENERATOR
30
NULL DETECTOR
32
ADC

Fig.1

10
12
SIGNAL CONDITIONING CIRCUIT
14
ADC
16
PROCESSOR
18
20
MEMORY
22
DISPLAY DEVICE
26
DUTY CYCLE CONTROL CIRCUIT
28
PULSE-WIDTH MODULATION CIRCUIT
30
NULL DETECTOR
32
ADC

Fig.2

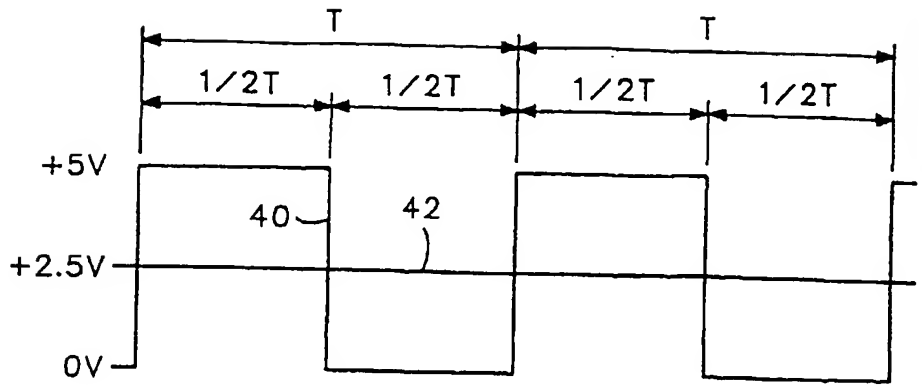

Fig.3A

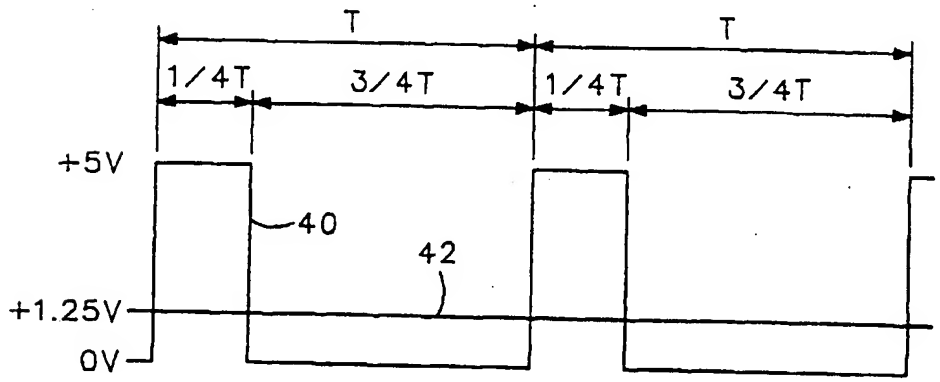

Fig.3B

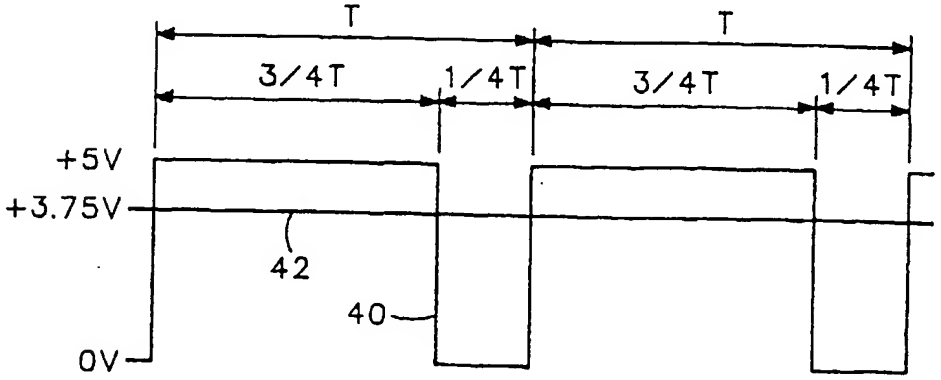

Fig.3C

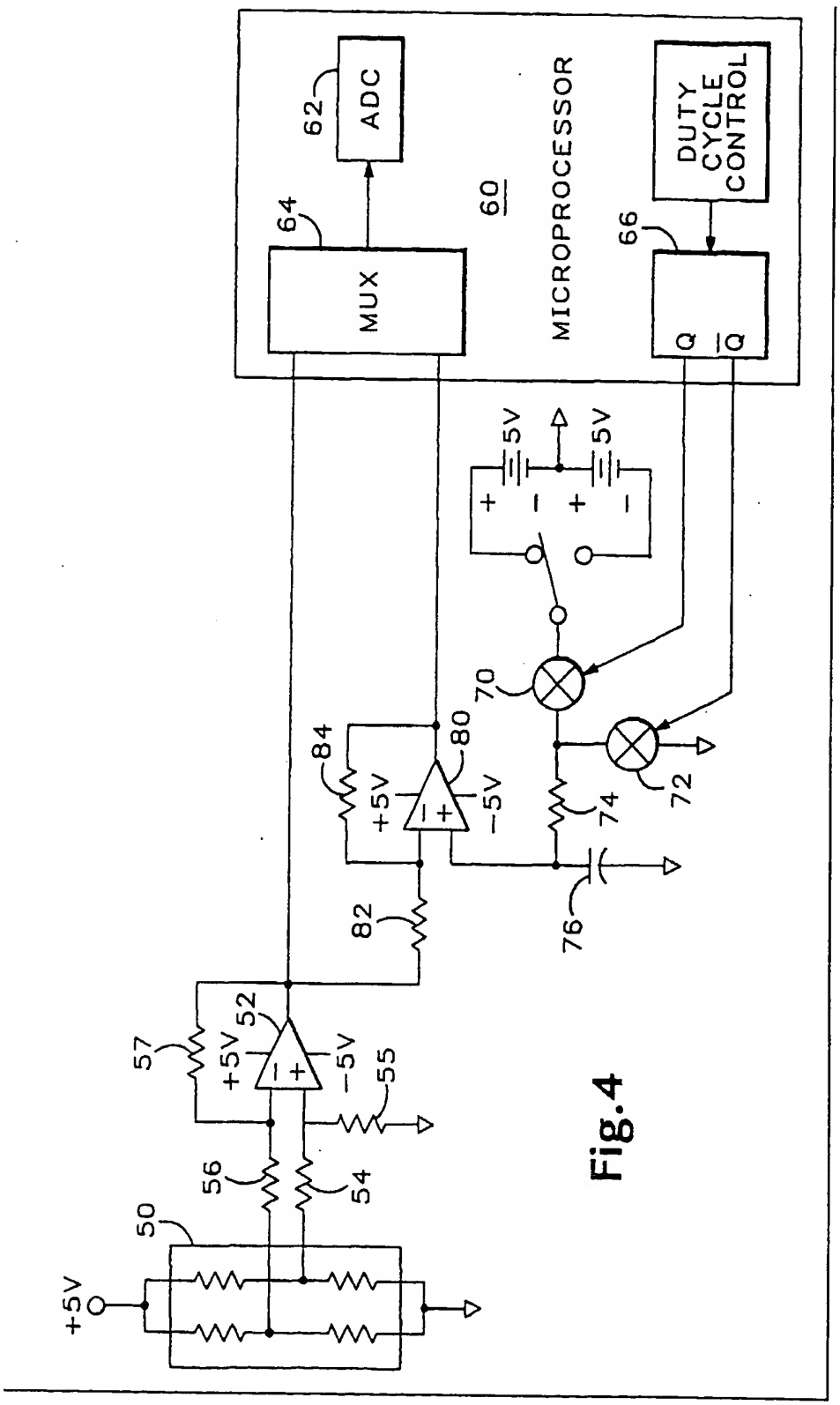
MICROPROCESSOR
60
ADC
62
MUX
64
DUTY CYCLE CONTROL
66
Q
Q
5V
5V
70
72
74
76
80
84
82
+5V
−5V
52
57
55
54
56
50
+5V

Fig.4

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(22) Date of filing: **29.11.1994**

(54) **Precision analog-to-digital converter with low-resolution and high-resolution conversion paths**

Präzisions-Analog-Digital-Umsetzer mit Umsetzungsstrecken niedriger und hoher Auflösung

Convertisseur analogique-numérique de précision comportant des voies de conversion à basse et haute résolution

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(56) References cited:
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EP-A- 0 072 144
DE-A- 4 312 697
US-A- 4 901 078

EP 0 683 567 B1

Description

Background of the Invention

[0001] This invention relates generally to analog-to-digital converters, and in particular to a precision analog-to-digital converter having low-resolution and high-resolution conversion paths.

[0002] There are many conventional analog-to-digital converters that are capable of measuring analog voltages with a high degree of precision. Most of these, however, are quite sophisticated, take up a great deal of space, consume a large amount of power, and are comparatively expensive. There are some measurement situations in which it would be desirable to provide a high-resolution analog-to-digital converter using relatively simple and inexpensive parts, and capable of implementation in a small area. One such situation, for example, is measurement of low-level signals from transducers, such as pressure transducers and the like, wherein it is desired to place a high-resolution analog-to-digital converter in a small module near the transducer and remote from the measuring instrument.

[0003] US-A-4 901 078 discloses an analog-to-digital converter which is arranged first to convert an input voltage into a digital value using a high-resolution recirculating-remainder A/D converter operated as a window detector. The input scaling is adjusted on the basis of the output of the window detector. The digital conversion is then repeated. Based on the output thereof, a signal generator produces a DC voltage which differs from the scaled input voltage by about $1/100^{th}$ of the dynamic range of the window detector. This difference is amplified by a low gain difference amplifier, and the output is then delivered to the window detector to produce a further digital value, which is combined with the value used to generate the DC voltage in order to obtain a representation of the input voltage.

Summary of the Invention

[0004] Aspects of the present invention are set out in the accompanying claims.

[0005] In one embodiment, a comparatively low-resolution (e.g., 4 bits or 8 bits) analog-to-digital converter (ADC) first converts an input signal to digital form to provide a first measurement. A first converted voltage for a 4-bit ADC is within 6.25% of the actual value of the input signal; for an 8-bit ADC, the converted voltage is within 0.4% of the actual value of the input signal. This value is utilized to establish the output DC voltage of a programmable precision DC voltage source, which DC voltage is applied to one input of a high-gain operational amplifier operated as a null detector, while the input signal is applied to the other input thereof. The sensitivity of the null detector is such that its output will be locked to one of its dynamic operating range limits, or saturated, if the voltage difference at its two inputs exceeds a predetermined voltage. In a preferred embodiment, a microprocessor stores the first-converted value, and then, using an 8-bit ADC, controls the duty cycle of a square-wave voltage signal that is applied to a low-pass filter to produce a pulse-width modulated direct-current (DC) voltage. That is, the precision DC voltage source produces a pulse-width-modulated DC voltage for application to one input of the high-gain operational amplifier. The gain of the operational amplifier is 500 so that the sensitivity is 20 millivolts for a 10-volt output swing (+5 V to -5 V).

[0006] Initially, the null detector is saturated, and its output voltage is clamped to a positive or negative supply voltage rail. The duty cycle of the switching signals is altered by the microprocessor to change the pulse-width modulated DC voltage until it is sufficiently close to the input signal to bring the null detector out of saturation and bring its output voltage within the dynamic operating range of the operational amplifier.

[0007] A binary search technique may be employed to adjust the duty cycle to locate a pulse-width modulated voltage which will either cause the null detector to come out of saturation or will be sufficiently close that a slight alteration in the duty cycle may be made to cause the null detector to come out of saturation. Alternatively, the first-converted value can be utilized to program a programmable counter to establish an initial duty cycle that can subsequently be varied one bit at a time until a pulse-width modulated voltage that causes the null detector to come out of saturation is reached. The first-converted value may be used to predict what the pulse-width modulated DC voltage should be so that the time taken to get the high-resolution measurement is slightly longer than the settling time of the pulse-width modulation circuit. Thus, the null detector comes out of saturation almost as soon as a pulse-width modulated DC voltage is developed, or after a few duty cycle adjustments, and output voltage thereof then may be converted to digital form to provide a second measurement, again using a low-resolution analog-to-digital converter. The output voltage of the null detector for the second measurement is between 0% and 0.4% of the input signal value when measured with an eight-bit analog-to-digital converter, as it was for the first measurement, and when added to the first-converted value (or a modified first-converted value used to establish the final duty cycle), yields a final value measured with an effective resolution of 18 to 22 bits of accuracy.

[0008] A preferred embodiment of the present invention is implemented in a measurement instrument for monitoring the analog voltage obtained from a commercially available pressure transducer. Signal conditioning is achieved using a precision instrumentation amplifier to match the output voltage range of the transducer with the measurement circuitry. A microprocessor including a simple 8-bit ADC is multiplexed between a low resolution (but high speed) reading and a fully settled reading of the null detector, which is rather slow, but produc-

es 18 to 22 bits of accuracy. The low-resolution reading is displayed to a user via a display device to give an indication of the measured input signal if the input signal is too noisy for the slower conversion to converge. A complete converged measurement process takes about a half a second to yield a high-resolution output, and can automatically sample and update the readings on a periodic basis.

[0009] The present invention can provide a simple, compact, low-cost, high-performance sampling analog-to-digital converter having a high-speed, low resolution conversion path, and a low-speed, high resolution conversion path.

Brief Description of the Drawings

[0010]

Fig. 1 is a generalized block diagram of an analog-to-digital converter in accordance with the present invention;

Fig. 2 is a block diagram of a preferred embodiment of the present invention;

Figs. 3A - 3C are waveforms to explain the operation of the pulse-width modulation technique employed by the preferred embodiment of the present invention; and

Fig. 4 is a schematic diagram of a preferred embodiment of the present invention.

Detailed Description of the Invention

[0011] Referring to Fig. 1 of the drawings, a generalized block diagram of an analog-to-digital converter (ADC) in accordance with the present invention is shown in which an input analog voltage to be measured is applied via an input terminal 10 to a signal conditioning circuit 12. Signal conditioning circuit 12 may be any conventional amplifier or attenuator, or a combination thereof, to condition and scale the input signal voltage to a suitable level for measurement within the conversion window or input range of the ADC.

[0012] The conditioned input voltage is applied to a comparatively low-resolution ADC 14, where it is converted to a digital representation. ADC 14 may be a simple 4-bit or 8-bit converter for first converting the input voltage to digital form to provide a first-converted voltage measurement. The first converted voltage for a 4-bit ADC is within 6.25% of the actual value of the input voltage; for an 8-bit ADC, the converted voltage is within 0.4% of the actual value of the input voltage.

[0013] A microprocessor 16 reads the output of ADC 14 and transports the digital representation of the amplitude, plus polarity sign, over a conventional microprocessor bus structure 18 to a memory device 20, which may suitably include a random-access memory (RAM) as well as a read-only memory (ROM) for storing programmed instructions, and to a display device 22, where it is immediately available to a user. Display device 22 may be any of a number of conventional display devices, such as a flat panel liquid crystal display (LCD) or the like.

[0014] Microprocessor 16 also initiates a programmable precision DC voltage generator 24, which may suitably be any of a number of well known programmable voltage sources, such as a digital-to-analog converter. The digital representation of the input voltage may be used by microprocessor 16 to initiate the voltage generator 24 to immediately produce a DC voltage near the input voltage being measured. The DC voltage is applied to one input of a null detector 30, which may be a high-gain operational amplifier, while the input signal is applied to the other input thereof. The output of null detector 30 is applied to a second ADC 32, which may be identical to ADC 14.

[0015] Initially, the null detector 30 is saturated, and its output voltage is clamped to a positive or negative supply voltage rail, such as +5 volts and -5 volts, which are the limits of its dynamic operating range. Microprocessor 16 reads the output of ADC 32, which indicates the saturated state of null detector 30, and alters the programming data applied over bus 18 to the precision DC voltage generator to change the DC voltage applied to null detector 30 until it is sufficiently close to the input voltage to bring null detector 30 out of saturation and bring its output voltage within the dynamic operating range of the operational amplifier.

[0016] Microprocessor 16 detects the unsaturated state of null detector 30 via ADC 32 and reads the second converted digital representation. The gain of the operational amplifier in null detector 30 may be such that the output voltage window provided by null detector 30 can interpolate between discrete conversion levels of ADC 14. This situation permits simply adding the second reading provided by ADC 32 to the first reading provided by ADC 14 to produce a final value. In any case, the programmed DC voltage, known to microprocessor 16 which caused such voltage to be generated, is added to the value measured by ADC 32 to provide a very precise representation of the unknown input voltage, with an effective resolution of 18 to 22 bits of accuracy. The final value then may be displayed to the user by display device 22. The final reading may take about a half a second to obtain, and can be updated on a periodic basis, for example, every second.

[0017] The first-converted value may be used to predict what the programmable DC voltage should be, and accordingly utilized to initialize the programmable precision DC voltage generator 24. Thereafter, a binary search technique may be employed to adjust the program data applied to voltage generator 24 to locate a DC voltage which will cause null detector 30 to come out of saturation. Alternatively, the program data can be varied one bit at a time until a DC voltage that causes null detector 30 to come out of saturation is reached. Thus, null detector 30 comes out of saturation almost

as soon as a DC voltage is developed, or after a few adjustments, and the output voltage thereof then may be converted to digital form to provide a second conversion measurement, again using a low-resolution analog-to-digital converter. The output voltage of the null detector for the fine measurement is between 0% and 0.4% of the input signal value when measured with an eight-bit analog-to-digital converter, and when added to the first-converted value (or a modified first-converted value used to establish the final duty cycle), yields a final value measured with an effective resolution of 18 to 22 bits of accuracy.

[0018] A preferred embodiment of the present invention is shown in block diagram form in Fig. 2, wherein like reference numerals are used for like elements. Here, the precision DC voltage source 24 is replaced by a duty-cycle control circuit 26 which controls the duty cycle of a square-wave voltage signal that is applied to a low-pass filter in a pulse-width modulation circuit 28 to produce a pulse-width modulated direct-current (DC) voltage. The rest of the circuit elements operate substantially as described in connection with Fig. 1. Again, as discussed above in connection with Fig. 1, the digital representation of the input voltage may be used by microprocessor 16 to initiate the duty-cycle control circuit 24 to immediately approximate a pulse-width modulated DC voltage near the input voltage being measured. The pulse-width-modulated DC voltage is applied to one input of a high-gain operational amplifier of null detector 30, while the input signal is applied to the other input thereof. The null detector 30 operates as described above. The duty cycle of the switching signals is altered by the microprocessor 16 to change the pulse-width modulated DC voltage applied to null detector 30 until it is sufficiently close to the input voltage to bring null detector 30 out of saturation and bring its output voltage within the dynamic operating range of the operational amplifier.

[0019] The first-converted value may be used to predict what the pulse-width modulated DC voltage should be, and accordingly utilized to initialize the duty cycle. Thereafter, a binary search technique may be employed to adjust the duty cycle to locate a pulse-width modulated voltage which will cause null detector 30 to come out of saturation. Alternatively, the first-converted value can be utilized to program a programmable counter to establish an initial duty cycle that can subsequently be varied one bit at a time until a pulse-width modulated voltage that causes null detector 30 to come out of saturation is reached. In any case, the pulse-width modulated DC voltage can be adjusted very precisely and quickly by varying the duty cycle of the control signal. Thus, null detector 30 comes out of saturation almost as soon as a pulse-width modulated DC voltage is developed, or after a few duty cycle adjustments, and the output voltage thereof then may be converted to digital form to provide a second conversion measurement, again using a low-resolution analog-to-digital converter. The output voltage of the null detector for the fine measurement is between 0% and 0.4% of the input signal value when measured with an eight-bit analog-to-digital converter, and when added to the first-converted value (or a modified first-converted value used to establish the final duty cycle), yields a final value measured with an effective resolution of 18 to 22 bits of accuracy.

[0020] To gain an appreciation of how the pulse-width modulated DC voltage is developed by adjusting the duty cycle of a square-wave signal, refer to the waveform diagrams shown in Figs. 3A through 3C. In Fig. 3A, a square-wave signal 40 is shown having an amplitude that varies from zero volts (0 V) to an exemplary reference voltage of five volts (+5 V), and has a duty cycle of 50%. That is, over one cycle indicated by time T, the square-wave voltage is at +5 V one-half of the time, or ½T, and at 0 V one-half of the time, or ½T. When filtered, a pulse-width modulated DC voltage level 42 is produced which is equal to one-half of the amplitude of the square-wave voltage, or +2.5 volts. In Fig. 3B, the duty cycle is adjusted to 25%, so that the square-wave signal voltage is at +5 V one-fourth of the time (¼T) and at 0 V three-fourths of the time (¾T), resulting in a pulse-width modulated DC voltage of +1.25 V. Similarly, in Fig. 3C, the duty cycle is adjusted to 75%, so that the square-wave signal voltage is at +5 V three-fourths of the time (¾T) and at 0 V one-fourth of the time (¼T), resulting in a pulse-width modulated DC voltage of +3.75 V. Thus, it can be discerned that the pulse-width modulated DC voltage 42 is proportional to the duty cycle of the control signal 40. For example, if a binary search sequence is used to adjust the pulse-width modulated DC voltage 42, the duty cycle may be first set to 50%, or to a percentage proportional to the value of the first reading by ADC 14, then the output of null detector 30 read to determine its state. Thereafter, the duty cycle can be adjusted to develop a pulse-width modulated DC voltage that converges toward the voltage of the input voltage in a well-known binary sequence V±½V±¼V±1/8V,etc., until the output of the null detector 30 comes out of saturation. It should be pointed out that while a positive polarity is used in this example, the principles described herein are identical for negative-polarity voltages.

[0021] Fig. 4 shows a preferred embodiment of the present invention as implemented to monitor the analog voltage from a commercially available pressure transducer 50 connected between a reference voltage of +5 V and ground. Pressure transducer 50 may be monitoring air pressure in an air line, for example. As pressure varies, a differential voltage is developed across internal resistances and applied to a signal conditioning stage comprising a precision instrumentation amplifier 52. Instrumentation amplifier 52 is configured as an operational amplifier to match the output range of the transducer with the measurement circuitry to condition the input signal, and in this embodiment has an output dynamic range of +5 volts to -5 volts. Resistors 54-57 associated with instrumentation amplifier 52 in this embod-

iment were selected to provide a gain of 40 for the signal conditioning stage.

[0022] The output of instrumentation amplifier 52, which is a replication of the input voltage, is applied directly to a microprocessor 60, which couples the replicated input voltage to an internal 8-bit ADC 62 via a multiplexer 64. One microprocessor capable of performing the functions described herein is a Hitachi H8-327 microprocessor. A duty-cycle control circuit 66, which may suitably be a variable duty cycle flip flop, provides complementary control signals at a one-kilohertz rate to operate a pair of switches 70 and 72, which alternately connect one end of a resistor 74 to a precise +5 V or -5 V reference, depending on the polarity of the input voltage, and ground in order to generate a square wave voltage similar to that shown in Figs. 3A-3C. Resistor 74 and capacitor 76 form a low-pass filter which effectively integrates the square-wave voltage to produce a pulse-width modulated DC voltage as described hereinabove.

[0023] The pulse-width modulated DO voltage generated by resistor 74 and capacitor 76 is applied to one input of an operational amplifier 80 that is operated as a null detector. The output of instrumentation amplifier 52 is coupled to a second input of operational amplifier 80 via an input resistor 82. A gain-setting feedback resistor 84 coupled from the output of operational amplifier 80 to its second input completes the null detector, and resistors 82 and 84 are selected to provide a gain of 500. Thus the sensitivity of the null detector is very high, and a 20 millivolt difference between the two inputs thereof will result in 10-volt change in the output. Since the output limits of the null detector are +5 volts and -5 volts, an input difference of greater than 20 millivolts will saturate the null detector and hold the output at one of the two extremes. The output of the null detector or operational amplifier 80 is coupled via mulitiplexer 64 to ADC 62. Thus, a single ADC 62 may be used for both the low-resolution, or first reading and the high-resolution, or second reading. Otherwise, the overall circuit functions as described hereinabove, and microprocessor 60 including a simple 8-bit ADC 62 is multiplexed between a low resolution (but high speed) reading and a fully settled reading of the null detector, which is rather slow, but produces 18 to 22 bits of accuracy. The low-resolution reading is available immediately to a user via a display device to give an indication of the measured input signal while the slower conversion is taking place. The entire process takes about a half a second to yield a high-resolution output, and the system can automatically sample and update the readings on a periodic basis.

Claims

1. A voltage measurement circuit comprising:

   an input path for receiving an input voltage to be measured;

   analog-to-digital conversion means (14,32; 62) arranged for converting the input voltage to a first converted voltage;

   a processor circuit (16; 60) arranged for receiving said first converted voltage;

   a programmable DC voltage generator (24; 26,28; 66,70,72,74,76) arranged to provide a DC reference voltage having a level determined by the processor circuit (16; 60) the processor circuit (16; 60) determining a starting level from said first converted voltage;

   difference means (30; 80,82,84) having a first input coupled to said input path, a second input coupled to an output of said programmable DC voltage generator (24; 26,28; 66,70,72,74,76) and an output coupled to said analog-to-digital conversion means (14,32; 62), the difference means (30; 80,82,84) being operable to provide at its output a difference signal representing the difference between the levels at its inputs, and the analog-to-digital conversion means (14,32; 62) being operable to convert the difference signal to a second converted voltage;

   said processor circuit (16; 60) being operable to combine the second converted voltage with the first converted voltage used to provide the DC reference voltage to provide a final converted voltage representative of said input voltage;

   characterised in that:

   said difference means comprises a null detector (30; 80,82,84) which provides said difference signal only when the voltages at its first and second inputs are substantially equal; and

   said processor circuit (16; 60) is arranged to monitor an output of the analog-to-digital converter means (14,32; 62) while altering the first converted voltage to command the programmable DC voltage generator (24; 26,28; 66,70,72,74,76) to adjust said DC reference voltage until the output of said null detector (30; 80,82,84) indicates that the voltages at its first and second inputs are substantially equal.

2. A voltage measurement circuit in accordance with claim 1 wherein said processor circuit is operable to perform a binary search to establish a value for said DC reference voltage.

3. A voltage measurement circuit in accordance with claim 1 or 2 wherein said analog-to-digital conversion means is a single analog-to-digital converter (62) selectively coupled to said input path and said output of said null detector (80,82,84).

4. A voltage measurement circuit in accordance with claim 1 or 2 wherein said analog-to-digital conver-

sion means comprises a first analog-to-digital converter (14) coupled to said input path and a second analog-to-digital converter (32) coupled to the output of said null detector.

5. A voltage measurement circuit in accordance with any preceding claim wherein said first converted voltage and said final converted voltage are provided to a display device (22).

6. A voltage measurement circuit in accordance with any preceding claim wherein said programmable DC voltage generator comprises a pulse width modulation circuit (28; 70,72,74,76) which produces said DC reference voltage in response to a square-wave voltage signal, and further wherein said processor (16; 60) varies the duty cycle of said square-wave voltage signal.

7. A voltage measurement circuit in accordance with any preceding claim wherein said null detector is an operational amplifier (80) having a predetermined gain.

8. A method of converting an input voltage to a digital signal, the method comprising performing an initial conversion of said input voltage to obtain a first, relatively low-resolution digital value, using said first digital value to generate a corresponding analog voltage, comparing the input voltage with said analog voltage and converting the difference therebetween to a second digital value, and providing a third, relatively high-resolution digital value as a representation of the input voltage;

characterised by the step of adjusting the first digital value until the comparison of the input voltage with the analog voltage indicates that they are substantially equal, the third digital value being based on the combination of the adjusted first digital value and the second digital value.

Patentansprüche

1. Spannungsmeßschaltung mit

einem Eingangsweg zum Empfang einer zu messenden Eingangsspannung,
einer Analog-Digital-Umwandlungseinrichtung (14, 32; 62) zur Umwandlung der Eingangsspannung in eine erste umgewandelte Spannung,
einer Verarbeitungseinheit (16; 60) zum Empfang der ersten umgewandelten Spannung,
einer programmierbaren Gleichspannungserzeugungseinrichtung (24; 26, 28; 66, 70, 72, 74, 76) zur Bereitstellung einer Gleichspannung-Referenzspannung mit einem durch die Verarbeitungsschaltung (16; 60) bestimmten Pegel, wobei die Verarbeitungsschaltung (16; 60) einen Startpegel von der ersten umgewandelten Spannung bestimmt,
einer Differenzeinrichtung (30; 80, 82, 84) mit einem ersten Eingangsanschluß, der an den Eingangsweg angeschlossen ist, einem zweiten Eingangsanschluß, der an einen Ausgangsanschluß der programmierbaren Gleichspannungserzeugungseinrichtung (24; 26, 28; 66, 70, 72, 74, 76) angeschlossen ist, und einem Ausgangsanschluß, der an die Analog-Digital-Umwandlungseinrichtung (14, 32; 62) angeschlossen ist, wobei die Differenzeinrichtung (30; 80, 82, 84) zur Bereitstellung eines Differenzsignals an ihrem Ausgangsanschluß betreibbar ist, das die Differenz zwischen den Pegeln an ihren Eingangsanschlüssen darstellt, und die Analog-Digital-Umwandlungseinrichtung (14, 32; 62) zur Umwandlung des Differenzsignals in eine zweite umgewandelte Spannung betreibbar ist,
wobei die Verarbeitungsschaltung (16; 60) zur Kombinierung der zweiten umgewandelten Spannung mit der ersten umgewandelten Spannung, die zur Bereitstellung der Gleichspannung-Referenzspannung verwendet wird, betreibbar ist, damit eine umgewandelte Endspannung bereitgestellt wird, die die Eingangsspannung darstellt,

dadurch gekennzeichnet, daß

die Differenzeinrichtung eine Null-Erfassungseinheit (30; 80, 82, 84) aufweist, die das Differenzsignal lediglich dann bereitstellt, wenn die Spannungen an ihren ersten und zweiten Eingangsanschlüssen im wesentlichen gleich sind, und
die Verarbeitungsschaltung (16, 60) eingerichtet ist, ein Ausgangssignal der Analog-Digital-Umwandlungseinrichtung (14, 32; 62) zu überwachen, während die erste umgewandelte Spannung verändert wird, damit die programmierbare Gleichspannungserzeugungseinrichtung (24; 26, 28; 66, 70, 72, 74, 76) angewiesen wird, die Gleichspannung-Referenzspannung anzupassen, bis das Ausgangssignal der Null-Erfassungseinheit (30; 80, 82, 84) anzeigt, daß die Spannungen an ihren ersten und zweiten Eingangsanschlüssen im wesentlichen gleich sind.

2. Spannungsmeßschaltung nach Anspruch 1, wobei die Verarbeitungsschaltung zur Ausführung einer binären Suche zur Bildung eines Werts für die Gleichspannung-Referenzspannung betreibbar ist.

3. Spannungsmeßschaltung nach Anspruch 1 oder 2, wobei die Analog-Digital-Umwandlungseinrichtung eine einzelne Analog-Digital-Umwandlungseinheit (62) ist, die selektiv an den Eingangsweg und den Ausgangsanschluß der Null-Erfassungseinheit (80, 82, 84) angeschlossen wird.

4. Spannungsmeßschaltung nach Anspruch 1 oder 2, wobei die Analog-Digital-Umwandlungseinrichtung eine erste Analog-Digital-Umwandlungseinheit (14), die an den Eingangsweg angeschlossen ist, und eine zweite Analog-Digital-Umwandlungseinheit (32) umfaßt, die an den Ausgangsanschluß der Null-Erfassungseinheit angeschlossen ist.

5. Spannungsmeßschaltung nach zumindest einem der vorhergehenden Ansprüche, wobei die erste umgewandelte Spannung und die umgewandelte Endspannung bei einer Anzeigevorrichtung (22) bereitgestellt werden.

6. Spannungsmeßschaltung nach zumindest einem der vorhergehenden Ansprüche, wobei die programmierbare Gleichspannungserzeugungseinrichtung eine Impulsbreitenmodulationsschaltung (28; 70, 72, 74, 76) aufweist, die die Gleichspannung-Referenzspannung in Reaktion auf ein Rechteckspannungssignal erzeugt, und ferner die Verarbeitungsschaltung (16; 60) das Tastverhältnis des Rechteckspannungssignals variiert.

7. Spannungsmeßschaltung nach zumindest einem der vorhergehenden Ansprüche, wobei die Null-Erfassungseinheit ein Operationsverstärker (80) mit einer vorbestimmten Verstärkung ist.

8. Verfahren zum Umwandeln einer Eingangsspannung in ein digitales Signal, mit den Schritten Ausführen einer Anfangsumwandlung der Eingangsspannung, damit ein erster digitaler Wert mit relativ niedriger Auflösung erhalten wird, Verwenden des ersten digitalen Werts zur Erzeugung einer entsprechenden analogen Spannung, Vergleichen der Eingangsspannung mit der analogen Spannung sowie Umwandeln der Differenz zwischen den Spannungen in einen zweiten digitalen Wert und Bereitstellen eines dritten digitalen Werts mit relativ hoher Auflösung als Darstellung der Eingangsspannung,

gekennzeichnet durch einen Schritt zum Anpassen des ersten digitalen Werts, bis der Vergleich der Eingangsspannung mit der analogen Spannung anzeigt, daß sie im wesentlichen gleich sind, wobei der dritte digitale Wert auf der Kombination des angepaßten ersten digitalen Werts und des zweiten digitalen Werts beruht.

Revendications

1. Circuit de mesure de tension comprenant :

un trajet d'entrée destiné à la réception d'une tension d'entrée à mesurer ;
un moyen de conversion analogique-numérique (14, 32 ; 62) disposé de manière à convertir la tension d'entrée en une première tension convertie ;
un circuit processeur (16 ; 60) disposé de manière à recevoir ladite première tension convertie ;
un générateur de tension continue programmable (24 ; 26, 28 ; 66, 70, 72, 74, 76), disposé de manière à produire une tension de référence continue ayant un niveau déterminé par le circuit processeur (16 ; 60), le circuit processeur (16 ; 60) déterminant un niveau de départ de ladite première tension convertie ;
un moyen de différence (30 ; 80, 82, 84) ayant une première entrée couplée audit trajet d'entrée, une seconde entrée couplée à une sortie dudit générateur de tension continue programmable (24 ; 26, 28 ; 66, 70, 72, 74, 76) et une sortie couplée audit moyen de conversion analogique-numérique (14, 32 ; 62), le moyen de différence (30 ; 80, 82, 84) étant activable afin de produire sur sa sortie un signal différentiel représentant la différence entre les niveaux de ses sorties et le moyen de conversion analogique-numérique (14, 32 ; 62) étant activable afin de convertir le signal de différence en une seconde tension convertie ;
ledit circuit processeur (16 ; 60) étant activable afin de combiner la seconde tension convertie avec la première tension convertie servant à produire la tension de référence continue afin de produire une tension finale convertie représentative de ladite tension d'entrée ;

caractérisé en ce que :

ledit moyen de différence comprend un détecteur de zéro (30 ; 80, 82, 84) ne produisant ledit signal de différence que lorsque les tensions de ses première et seconde entrées sont pratiquement égales ; et
ledit circuit processeur (16 ; 60) est disposé afin de surveiller une sortie du moyen de conversion analogique-numérique (14, 32 ; 62) tout en modifiant la première tension convertie pour commander le générateur de tension continue programmable (24 ; 26, 28 ; 66, 70, 72, 74, 76) afin d'ajuster ladite tension de référence continue jusqu'à ce que la sortie dudit détecteur de zéro (30 ; 80, 82, 84) indique que les tensions de ses première et seconde entrées sont pra-

tiquement égales.

2. Circuit de mesure de tension selon la revendication 1 dans lequel ledit circuit processeur est activable pour procéder à une recherche binaire afin d'établir une valeur pour ladite tension de référence continue.

3. Circuit de mesure de tension selon la revendication 1 ou 2, dans lequel ledit moyen de conversion analogique-numérique est un convertisseur analogique-numérique unique (62) couplé de manière sélective audit trajet d'entrée et à ladite sortie dudit détecteur de zéro (80, 82, 84).

4. Circuit de mesure de tension selon la revendication 1 ou la revendication 2 dans lequel ledit moyen de conversion analogique-numérique comprend un premier convertisseur analogique-numérique (14) couplé audit trajet d'entrée et un second convertisseur analogique-numérique (32) couplé à la sortie dudit détecteur de zéro.

5. Circuit de mesure de tension selon l'une quelconque des revendications précédentes dans lequel ladite première tension convertie et ladite tension finale convertie sont appliquées à un dispositif d'affichage (22).

6. Circuit de mesure de tension selon l'une quelconque des revendications précédentes, dans lequel ledit générateur de tension continue programmable comprend un circuit de modulation de largeur d'impulsion (28 ; 70, 72, 74, 76) produisant ladite tension de référence continue en réponse à un signal de tension de forme carrée, et dans lequel, en outre, ledit processeur (16 ; 60) fait varier le cycle du rapport cyclique dudit signal de tension de forme carrée.

7. Circuit de mesure de tension selon l'une quelconque des revendications précédentes dans lequel ledit détecteur de zéro est un amplificateur opérationnel (80) de gain prédéterminé.

8. Procédé de conversion d'une tension d'entrée en un signal numérique, le procédé comprenant la mise en oeuvre d'une conversion initiale de ladite tension d'entrée afin d'obtenir une première valeur numérique de résolution relativement faible, l'utilisation de la dite première valeur numérique pour générer une tension analogique correspondante, la comparaison de la tension d'entrée à ladite tension analogique et la conversion de leur différence en une seconde valeur numérique et la production d'une troisième valeur de résolution relativement élevée comme représentation de la tension d'entrée ;

caractérisé par l'étape d'ajustement de la première valeur numérique jusqu'à ce que la comparaison de la tension d'entrée avec la tension analogique indique qu'elles sont pratiquement égales, la troisième valeur numérique étant basée sur la combinaison de la première valeur numérique ajustée et de la seconde valeur numérique.

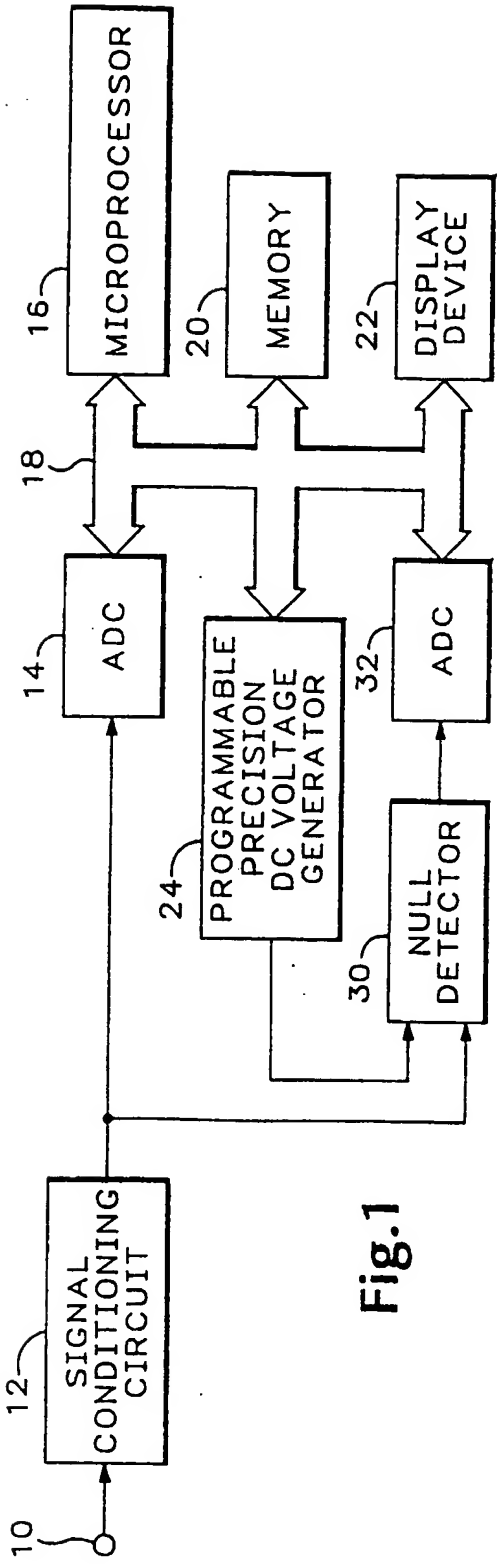
10
SIGNAL CONDITIONING CIRCUIT
12
ADC
14
18
MICROPROCESSOR
16
MEMORY
20
DISPLAY DEVICE
22
PROGRAMMABLE PRECISION DC VOLTAGE GENERATOR
24
ADC
32
NULL DETECTOR
30

Fig.1

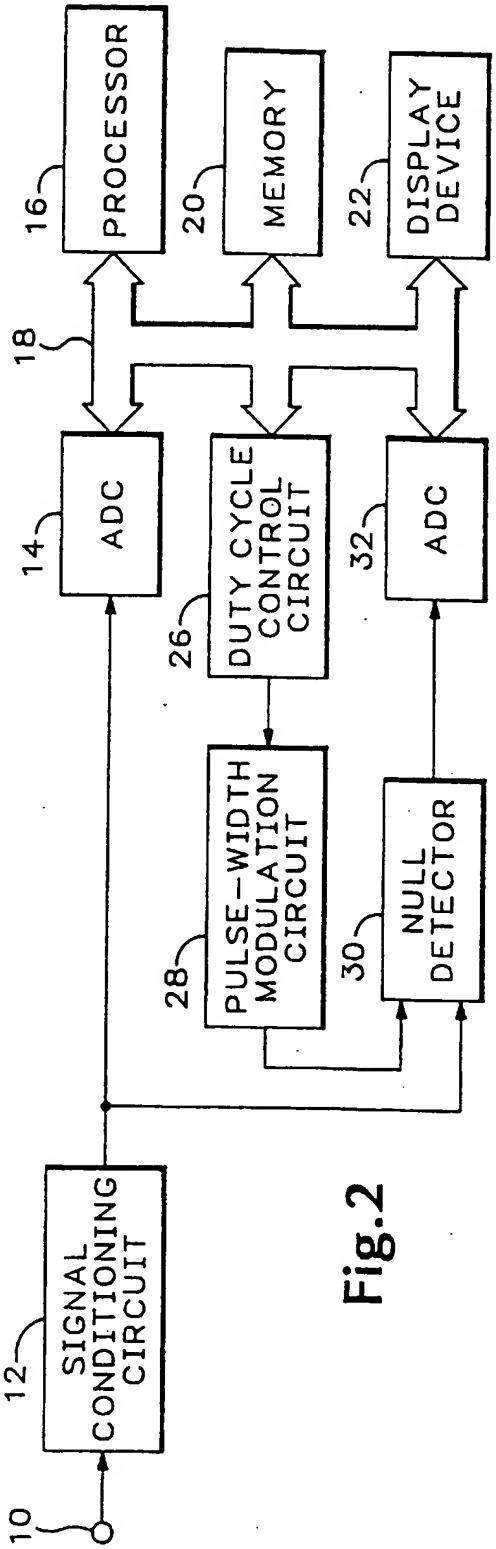
10
SIGNAL CONDITIONING CIRCUIT
12
ADC
14
18
PROCESSOR
16
MEMORY
20
DISPLAY DEVICE
22
DUTY CYCLE CONTROL CIRCUIT
26
PULSE-WIDTH MODULATION CIRCUIT
28
ADC
32
NULL DETECTOR
30

Fig.2

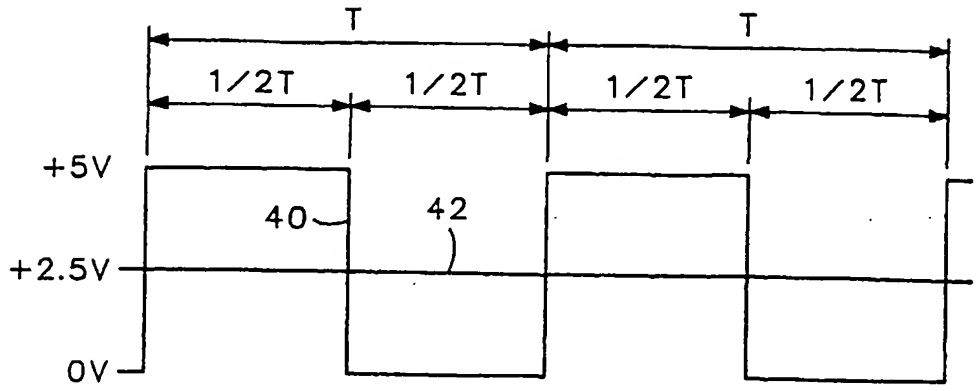

Fig.3A

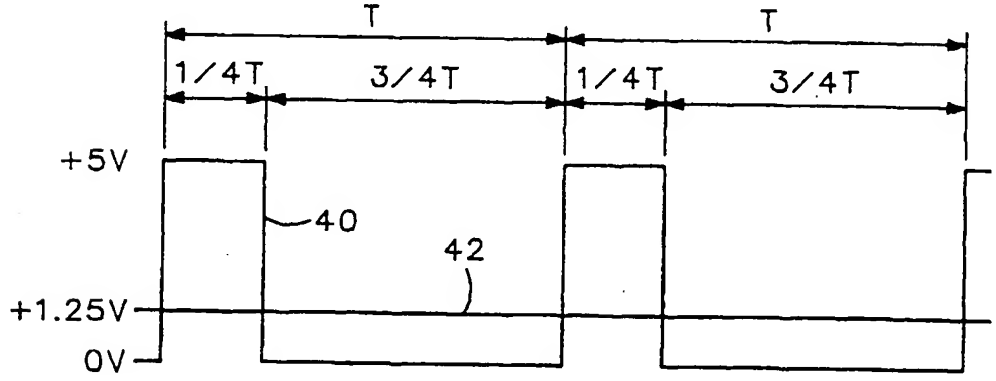

Fig.3B

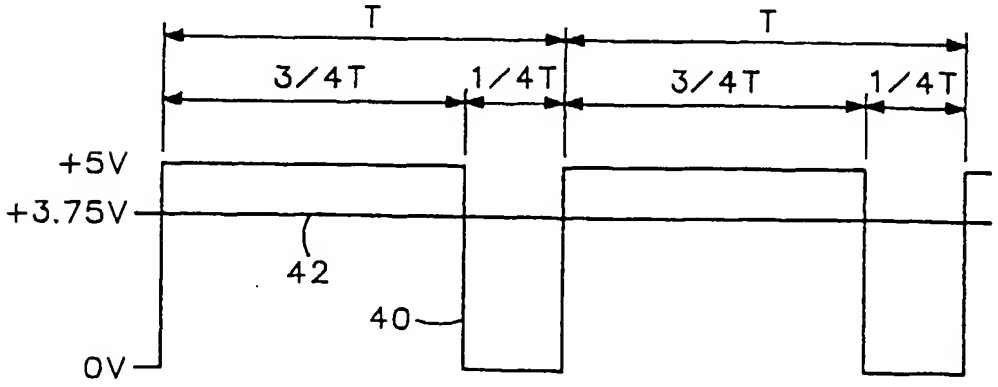

Fig.3C

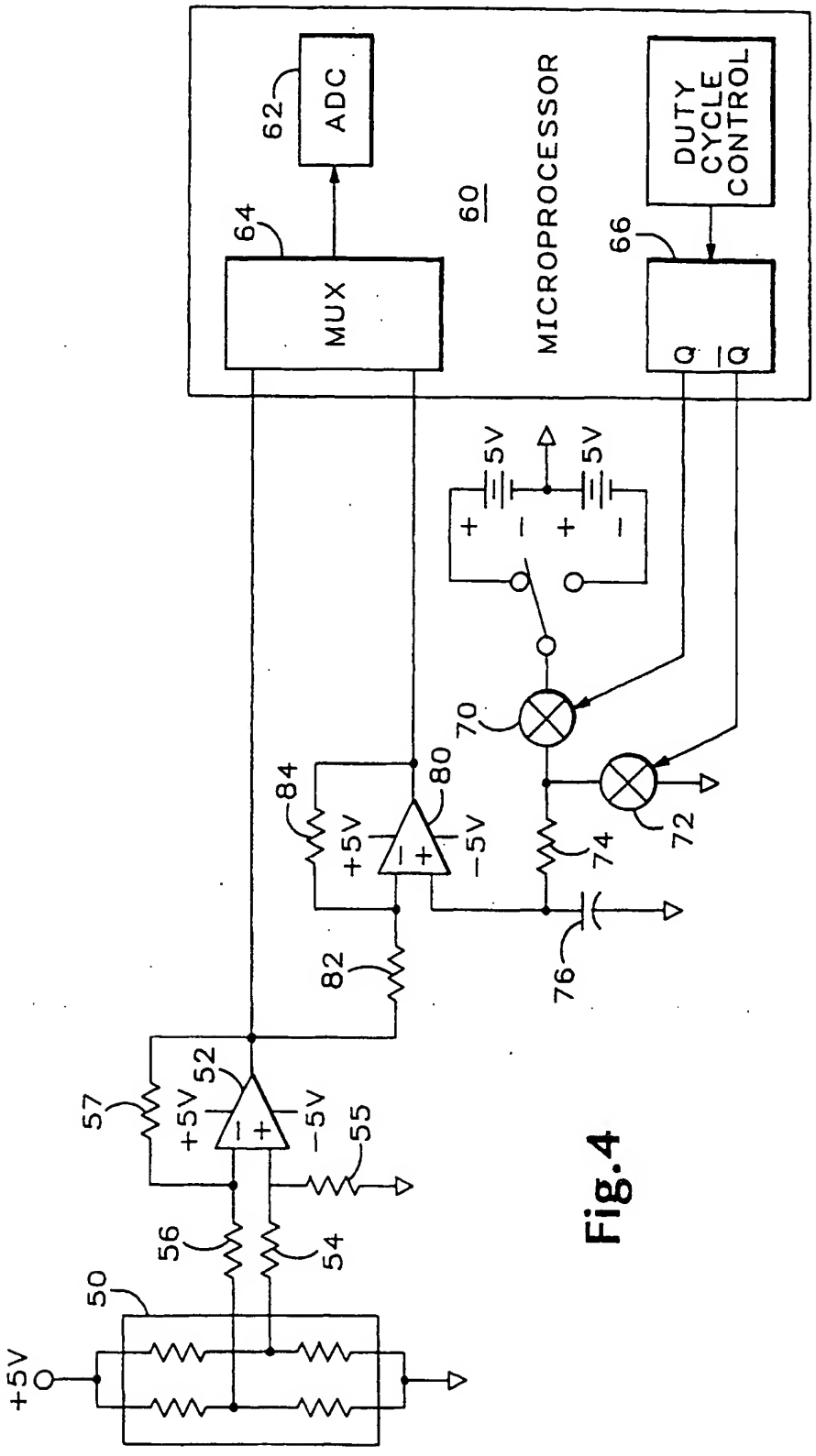
MICROPROCESSOR
60
ADC
62
MUX
64
DUTY CYCLE CONTROL
66
Q
Q
5V
5V
70
72
74
76
80
84
+5V
-5V
82
52
57
+5V
-5V
55
56
54
50
+5V

Fig.4